EE 435 Name_____
Final Exam
Spring 2025

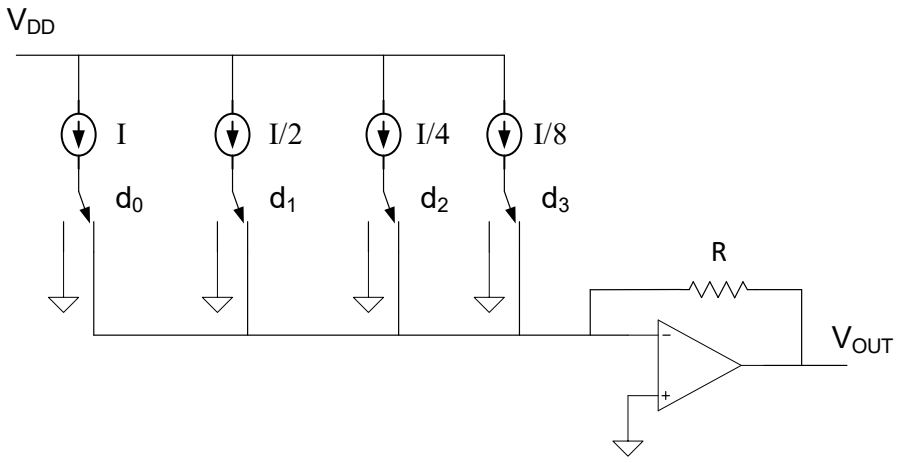
Instructions: This is an open-book, open-notes exam. It is due at 9:30 a.m. on Wednesday May 14. Print this exam and provide solutions directly on the printed exam. Add additional pages if more space is needed for completing your solutions. The solutions should be slid under the office door of the course instructor (Room 2133 Coover). On those problems that need technology parameters, assume you are working in a 0.18μm CMOS process with key parameters $\mu_n C_{OX}=250\mu A/v^2$, $\mu_p C_{OX}=\mu_n C_{OX}/3$, $V_{TNO}=0.4V$, $V_{TPO}= - 0.4V$, $C_{OX}=2fF/\mu^2$, $\lambda =0.01v^{-1}$, $\gamma = 0$, Cbdbot = $0.5fF/\mu^2$, and Cbdsw = $2.5fF/\mu$.
All work is to be individual with no discussion with anyone else (except as specified below) , no posting of the exam questions, and no use of any other source for obtaining the solutions (such as Chegg) of the problems. You may make unlimited use of WEB resources for obtaining technical information. You may consult the designated instructor of the course or the designated Teaching Assistant if you have questions. You will be expected to certify that you comply with the honor system by signing the following statement.

I certify that I completed this exam in compliance with the honor system described above _____ (signature).

Problem 1 Consider the DAC circuit shown below.

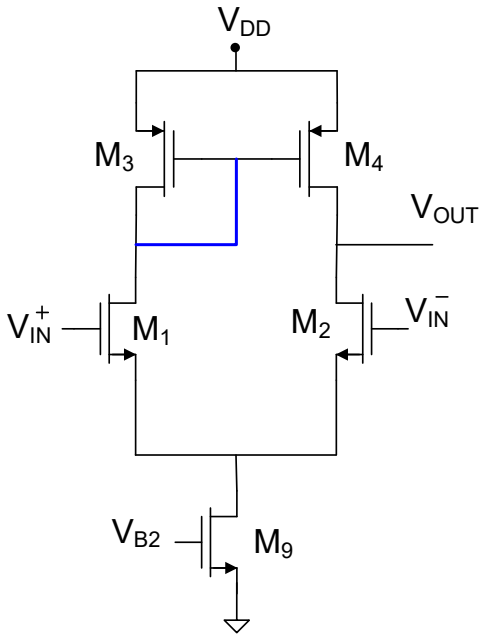
a) Derive an expression for the output voltage as a function of the Boolean inputs d_0, d_1, d_2 and d_3 and the circuit elements in the circuit. Assume all circuit elements shown are ideal and assume the op amp is ideal as well.

b) If the current source above the switch d_0 is 10% below the nominal (ideal) value and all other current sources are equal to their nominal values, determine the INL of this DAC.



Problem 2 Assume in your new job you were told that a previous engineer who worked for the company had designed a 5T op amp in the 0.18µm process (process parameters given in instructions of this exam) and that you were to first obtain the circuit schematic and then modify the design for a new project. But when you went to the design document on file, the only design information that was provided by the previous engineer was a note that the magnitude of all of the excess bias voltages were the same and that the op amp was to operate with a supply voltage of 3.6V. There were also some rudimentary test results included. When a differential step input of 20uV was applied to the open-loop amplifier, a step on the output of 10mV was observed and that when a 1nF capacitor was placed on the output and a large step was applied to the differential input, it took 2usec for the voltage across the load capacitor to increase from 2V to 3V.

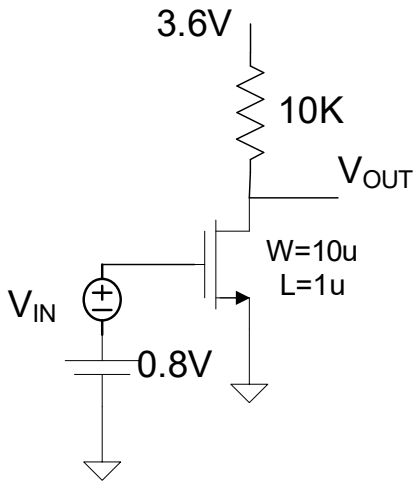
a) What is the power dissipation of the op amp?
b) What is the GB of the op amp?
c) What is W_1/L_1 ?
d) What is V_{B2} ?



Problem 3 A 12-bit string DAC has an INL of 10 LSB. Determine the ENOB from an INL perspective.

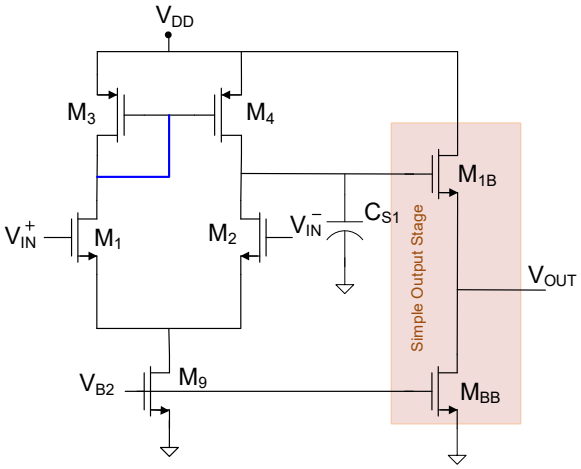
Problem 4 Consider the following circuit where $V_{IN} = 0.025\sin(2000\pi t)$

a) Determine V_{OUT}.
b) Determine the RMS output noise voltage at T=300K in the interval from dc to 10KHz. Include only the thermal noise in the load resistor and in the transistor in this calculation.
c) Determine the signal to noise ratio (SNR) at the output where the noise is that in the interval determined in part b)



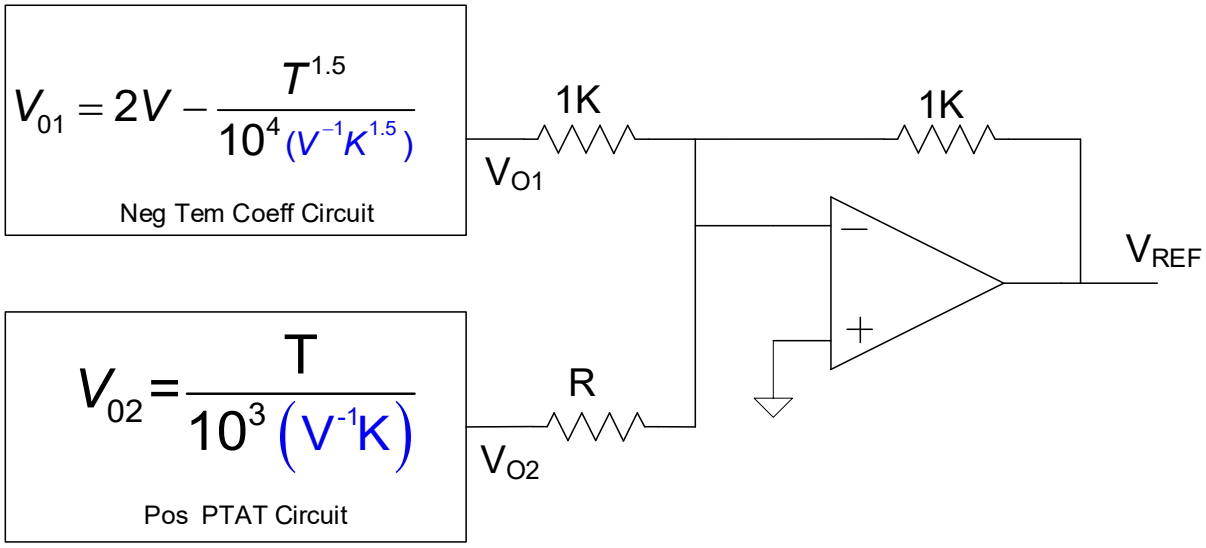
Problem 5 Consider the following amplifier which includes a simple output stage. Assume V_{DD}=3.6V, C_{S1}=2pF, and the circuit was designed so that all transistors have V_{EB}=0.2V. Further assume the total power dissipation is 10mW and that this power is split evenly between the differential stage and the output stage.

a) Determine W_1/L_1
b) Determine W_{1B}/L_{1B}
c) What is the maximum output signal swing?



Problem 6 The circuit shown has been proposed as a voltage reference. It has two temperature sensors, one with a positive temperature coefficient and the other with a negative temperature coefficient. (The two boxes on the left are assumed to be voltage sources with zero output impedance and output voltages given by the equations shown in the figure.)

a) Determine R so that the temperature coefficient of V_{REF} is 0 at T=300K.
b) With the value of R determined in part a), what is the maximum deviation in V_{REF} from the value output at 300K for 250K<T<350K?

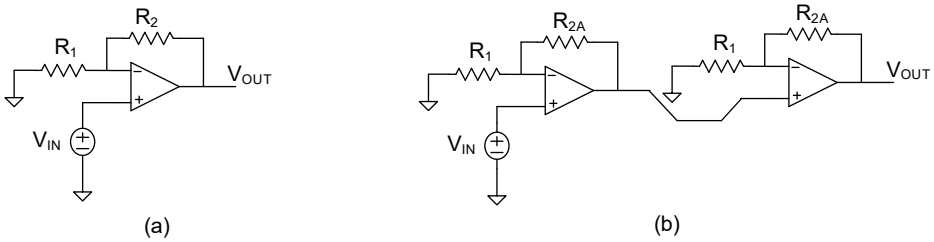


Problem 7 A periodic signal was applied to a DAC and the output was sampled 4096 times at 1msec spacings over precisely 11 periods of the output. A DFT using the FFT was used to obtain the DFT of the sampled sequence. The magnitude of the first 120 terms, expressed in DB, are given on the following page. All remaining terms were smaller than -95dB.

a) What is the magnitude of the signal?
b) What was the frequency of the signal?
c) What is the SFDR?
d) What is the THD?

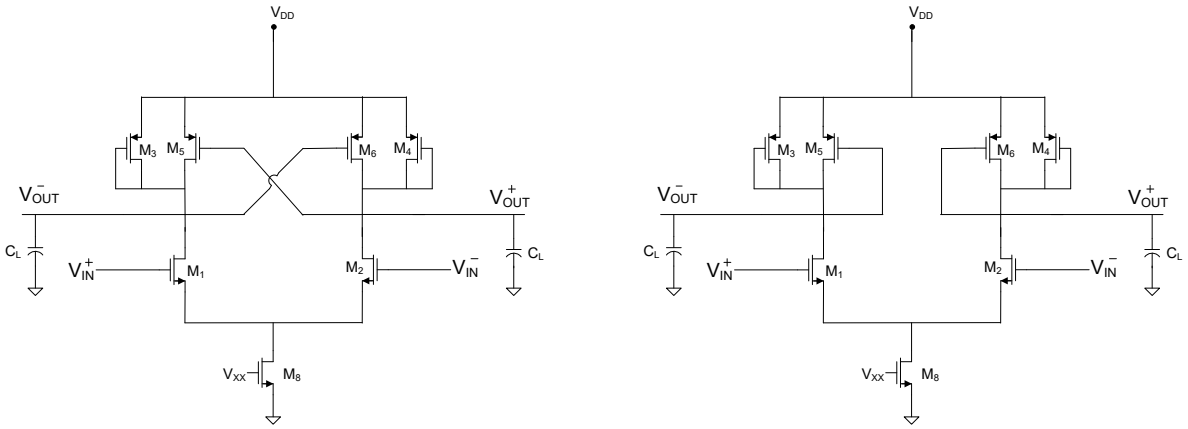
Index Number	Mag (dB)	Index Number	Mag (dB)	Index Number	Mag (dB)
1	-97.23	41	-99.21	81	-99.21
2	-98.4	42	-97.43	82	-97.43
3	-96.3	43	-95.61	83	-95.61
4	-99.21	44	-97.4	84	-97.4
5	-97.43	45	-97.23	85	-97.23
6	-95.61	46	-98.2	86	-98.2
7	-97.4	47	-99.4	87	-99.4
8	-97.23	48	-98.78	88	-98.78
9	-98.2	49	-99.21	89	-97.23
10	-99.4	50	-97.43	90	-99.21
11	-98.78	51	-95.61	91	-97.43
12	4.001	52	-97.4	92	-95.61
13	-96.3	53	-97.23	93	-97.4
14	-99.21	54	-98.2	94	-97.23
15	-97.43	55	-99.4	95	-98.2
16	-95.61	56	-98.78	96	-99.4
17	-97.4	57	-97.23	97	-98.78
18	-97.23	58	-98.4	98	-97.23
19	-98.2	59	-96.3	99	-98.4
20	-99.4	60	-99.21	100	-96.3
21	-98.78	61	-97.43	101	-99.21
22	-97.23	62	-95.61	102	-97.43
23	-57.2	63	-97.4	103	-95.61
24	-96.3	64	-98.78	104	-97.4
25	-99.21	65	-98.83	105	-98.78
26	-97.43	66	-96.3	106	-98.3
27	-95.61	67	-99.21	107	-96.3
28	-97.4	68	-97.23	108	-99.21
29	-98.78	69	-98.4	109	-97.43
30	-98.3	70	-96.3	110	-95.61
31	-96.3	71	-99.21	111	-97.4
32	-99.21	72	-97.43	112	-97.23
33	-97.43	73	-95.61	113	-97.23
34	-60.9	74	-97.4	114	-98.4
35	-97.4	75	-98.78	115	-96.3
36	-97.23	76	-98.3	116	-99.21
37	-98.2	77	-96.3	117	-97.43
38	-99.4	78	-99.21	118	-95.61
39	-98.78	79	-97.43	119	-97.4
40	-97.23	80	-95.61	120	-98.78

Problem 8 Operational amplifiers are often compensated for an acceptable transient response or gain peaking when connected in a standard feedback configuration such as shown in part (a) below. The consumer often uses the amplifier in other configurations. Shown below are two different amplifier structures. Assume that in all cases the resistors are chosen so that the dc gain of the feedback amplifier is 100. Assume the op amp has been designed so that it has a dc gain of 100,000 with a single left half-plane pole at -10 rad/sec. Analytically compare the 3dB bandwidth and the amplifier poles of the following circuits assuming the same op amp is used in both cases. Comment about the performance of the two different finite gain amplifiers (in this comparison, focus on whether the feedback amplifier will work, the corresponding closed-loop bandwidth, and any other factors you deem relevant in making a decision on which structure is most useful).



Problem 9 Two operational amplifiers are shown below. Assume the standard symmetry properties in both structures.

a) Compare the dc voltage gain (differential output voltage divided by the differential input voltage) of the two amplifiers in terms of the small-signal model parameters.
b) If the lengths of all devices are the same and $W_5=0.9W_3$, compare the dc voltage gain of the two amplifiers in terms of the natural design parameters.
c) Compare the power dissipation of the two amplifiers assuming the devices in the left circuit are sized identical to those in the right circuit.



Problem 10

Answer the following questions.

a) In a hybrid DAC architecture, the input is often partitioned into an MSB part and a LSB part. The MSB part of the input is often used as the input to a thermometer coded DAC and the LSB part of the input is often used as the input to a binary-coded DAC. What is the major reason this approach is often used?

b) In the bandgap circuits discussed in class, the ratio of the currents in the two diodes was kept constant independent of temperature. Why was this done?

c) What layout strategy is used to eliminate the effects of linear gradients in device parameters?

d) It was observed that a rapidly switched capacitor behaves as a resistor. Though this relationship was observed by Maxwell in the late 1800's, it was little more than an academic curiosity at the time. But in the late 1970's two important properties of circuits that used switched capacitors to implement resistors were recognized. What were those two important properties?

e) Miller compensation of an op amp was a major breakthrough but strict Miller compensation results in a zero on the positive real axis and this is undesirable. What simple circuit modification is often used to move the RHP zero to the negative real axis where performance of the circuit can actually be improved?

f) When compensating an op amp, dominant pole compensation is often used to move the pole on the output of the first stage to a very low frequency. Why is it not advantageous to also move the pole on the second stage to a lower frequency?

g) Switching currents on and off in a current-steering DAC causes large glitches on the output and long settling times to turn on and off the current sources. What strategy is used to dramatically reduce the glitches and settling time in current steering DACs?